Using wide bandgap devices for switched-mode power supplies

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***Abstract*—Devices using wide bandgap materials, such as Gallium nitride (GaN) are an upcomming technology for power supplies. But there are just a few devices designed for low power applications ($< 500W$) yet. This document points out the advantages and problems of using GaN and for what voltage ranges it is suitable.**

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Introduction

Switched-mode power supplies (SMPS) use semiconductor switches, to boost the frequency which means increasing inductive coupling and decreasing transformer sizes. There are different types regarding SMPS, for example:

- *server power supplies*: Designed for high stability and high efficiency (up to 96% and more)
- *laptop power supplies*: Designed to be cheap and compact (efficiency usually $< 90\%$)

This document focuses the role of wide bandgap (especially GaN) for building extremly compact 180 W laptop SMPS that converts from 230 V AC to 19.5 V DC. Such power supplies usually offer only one output voltage level, that is converted to lower levels on the laptop's mainboard. But this output has to handle big jitter and has to offer high voltage stability, as has been shown in corresponding work.[1] When designing laptop SMPS, the all over efficiency is not the main focus, but limited surface without active cooling forces compact power supplies, to be efficient.
There are different types of semiconductor switches, such as FETs, IGBTs or GTOs. Laptop SMPS operate at comperatively low currents and voltages, but on highest possible frequencies. Therefore FET-switches (MOS- or JFET) are the preferred technology. This devices can have a significant benefit from wide bandgap materials.

I. Power losses of transistors

There are two major types of transistor power losses regarding FETs:

- *conductive losses*
  - The energy, that is lost when the transistor is on, due to its on-resistance
  - Leakage currents when the transistor is off
- *switching losses*
  - driver losses: certain amount of energy necessary to load the gate capacity
  - turn-on/-off losses: energy lost, while the channel is not completely established

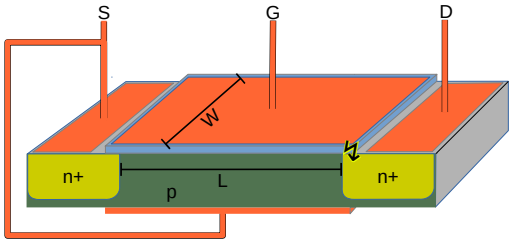

Fig. 1. Scematic of lateral NMOS FET (No PN-drift zone)

The on-resistance of a certain type of MOSFET is determined by the drift/channel length (L) and -width (W). The necessary drift length depends on material's breakdown field strength and the required drain to source blocking voltage.[4] To obtain a specified on-resistance, the width of the transistor has to be increased or more transistors have to be shut in parallel. But this means also increasing the gate capacity. Therefore the switching losses increase while conductive losses decrease. For each operating frequency and blocking voltage, a good trade-off between conductive losses and switching losses has to be found.

$$p_{\text{driver losses}} \sim W \cdot L \qquad p_{\text{conductive losses}} \sim \frac{L}{W}$$

With regard to this relations, comparing the specific on-resistances as function of blocking voltage of different materials is a meaningfull way, to show the particular's material's limits. Increasing the blocking voltage or the general conductivity both are options to enhance the total efficiency of a device.

II. Wide Bandgap

Wide bandgap means, that the forbidden gap (band gap) between valence band and conduction band is much higher (min. 1.7 eV) than the band gap of common semiconductors[2]. For building high efficient and compact power supplies the most important benefit of using wide bandgap devices is its higher breakdown voltage.

A. Blocking voltage

The maximum blocking voltage V_{BR} of power transistors is limited by the avalanche breakdown. Charge carriers moving

along the drift region can accumulate kinetic energy. Once they reach enough energy, a collision of moving carriers with valence band electrons can create a new electron-hole-pair (impact ionization). There is an impact ionization coefficient α that determins the statistical number of impact ionizations per moving carrier and cm.[25] This coefficient differs between electrons and holes, is temperature dependent, and can nearly be described for 300 K with:

$$\alpha_{\mathrm{n/p}} = a_{\mathrm{n/p}} \cdot e^{-\frac{b_{\mathrm{n/p}}}{E}}$$

The coefficients a and b are difficult to measure and given in table I.

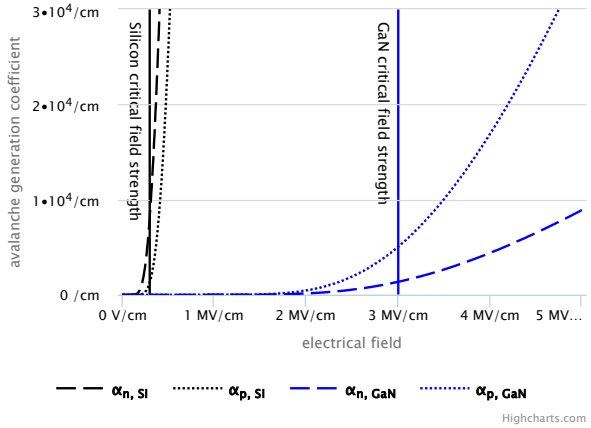

Fig. 2. Impact ionization coefficient for electrons and holes at 300 K

Whether a voltage, applied to a structure of semiconductor with length L, causes an avalanche breakdown depends on several factors. Assume $\alpha_{\mathrm{n}} = \alpha_{\mathrm{p}} = \alpha$. In this case, neglecting recombination, an electron-hole-pair created in the structure causes statistically

$$\int_0^L \alpha(x)\mathrm{d}x$$

impact ionizations, independently from the position at which the pair was created. The avalanche occurs, when this integral becomes ≥ 1.[26] α is dependent from x, because E may be dependent from x. There are two typical types of field gradients by applying a voltage V_{BR} to a structure of semiconductor. A homogeneous field $E(x) = \frac{V_{\mathrm{BR}}}{L}$ in case of an intrinsic semiconductor and a linear field $E(x) = \frac{2V_{\mathrm{BR}}}{L^2} \cdot x$ in case of a homogeneously doped semiconductor due to space charge region:

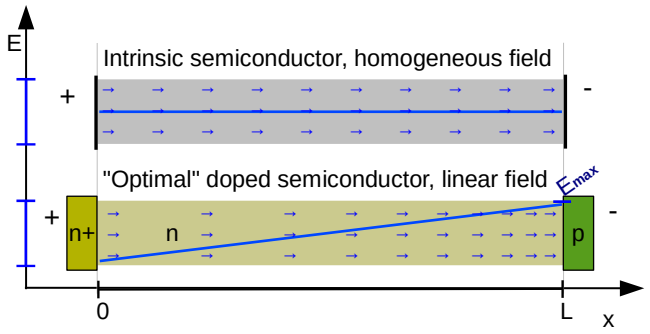

Fig. 3. Field strength gradients

If there is no inversion, each donator atom in the space charge region gives one electron and remains positively charged, so the gradient of the field strength depends on the dopant density. In optimal case, the field fills the complete structure without touching the n+ closure. This optimal dopant density is given by:

$$N_{\mathrm{D}} = \frac{2 \cdot \epsilon_0 \cdot \epsilon_r \cdot V_{\mathrm{BR}}}{q_0 \cdot L^2}$$

In case of the homogeneous field, the avalanche condition can be integrated and solved for V_{BR}, in case of linear field, this has to be done numerically.

$$\text{hom.: } V_{\mathrm{BR}} = \frac{b \cdot L}{ln(L \cdot a)} \quad \text{lin.: } \int_0^L a \cdot e^{-\frac{b \cdot L^2}{2 \cdot V_{\mathrm{BR}} \cdot x}} \mathrm{d}x - 1 = 0$$

This equations become even more complex, if one considers $\alpha_{\mathrm{n}} \neq \alpha_{\mathrm{p}}$. But computing the results for $\alpha = \alpha_{\mathrm{n}}$ and $\alpha = \alpha_{\mathrm{p}}$ independently and then taking the smaller value yields a good lower bound. Other methods use an effective avalanche coeffictent, usually described with a polynomial expression. This minimum voltage-length relations and its corresponding dopant density for the linear case are shown in the following chart:

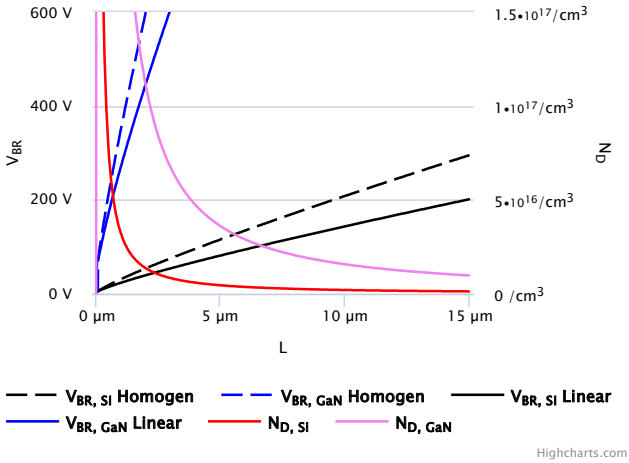

Fig. 4. Breakdown voltage and dopant density as a function of drift zone length at 300 K

B. Voltage-on-resistance relationship (linear field)

The resistivity of a n-type non-depleted semiconductor can be described with[13]

$$\rho = \frac{1}{q_0 \cdot \mu_\mathrm{n} \cdot N_\mathrm{D}} \qquad R_{\mathrm{DS,\,on}} \cdot A = \rho \cdot L = \frac{L^3}{2 \cdot \epsilon_0 \cdot \epsilon_r \cdot \mu_\mathrm{n} \cdot V_\mathrm{BR}}$$

The hole current and - mobility are negligible in n-type semiconductors. Latest GaN crystals got equal or even higher electron mobilities than silicon (Compare [6] - [9]).
Due to the strong non-linearity of $\alpha(E)$, the major avalanche generation happens in the high field strength edge. This maximum field strength of the linear field is given by $E_\mathrm{max} = \frac{2 \cdot V_\mathrm{BR}}{L}$. Therefore it is possible, to assume an upper bound critical field strength $E_\mathrm{max} = E_\mathrm{crit}$ as the avalanche condition. E_crit can approximately been given as a material constant, as shown in fig. 2. Using this simplification, the equation for the specific on-resistance can be written as:

$$R_{\mathrm{DS,\,on}} \cdot A = \frac{4 \cdot V_\mathrm{BR}^2}{\epsilon_0 \cdot \epsilon_r \cdot \mu_\mathrm{n} \cdot E_\mathrm{crit}^3}$$

It can be seen, that there is a factor $BFoM = \epsilon_r \cdot \mu_\mathrm{n} \cdot E_\mathrm{crit}^3$ (Baliga's figure of merit), that is well suited for comparing the blocking voltage - on-resistance relationships of different materials.[2]

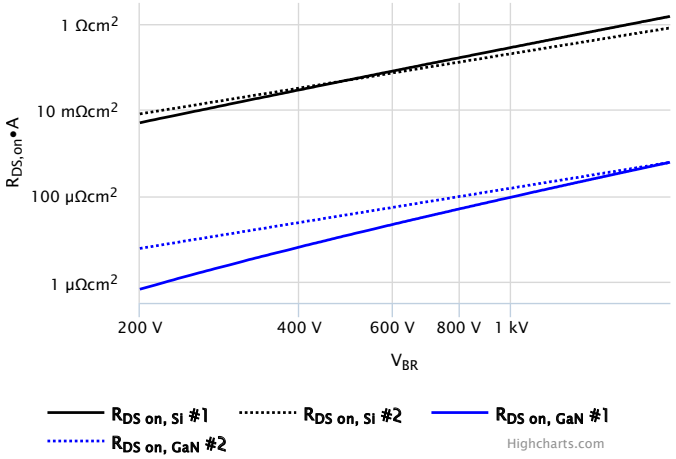

Fig. 5. Breakdown voltage - on-resistance relationship at 300 K
#1: numerical approximation with data from fig. 4
#2: simplification with constant E_crit

It should be said, that especially the GaN limit is not reachable for lower voltages, because the dopant density would degenerate the semiconductor. And of course this resistance is just the one of the doped drift region. When building real devices, there are several resistances, such as the channel or the packaging resistance. The silicon limit can be exceeded by super junction devices. Therefore GaN is suppressed by advanced silicon devices in the low voltage range.

C. MOSFET device topologies

To build a high power device, thats breakdown voltage - on-resistance ratio is near the derivated material's limit, a simple, scematic MOSFET as shown in fig. 1 is no option. A large, slightly doped n-drift region is required to hold the linear field:

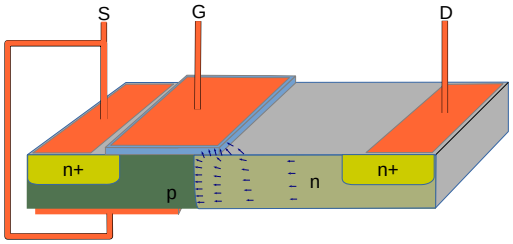

Fig. 6. Lateral NMOS

The field strength in the gate edge is still verry high in off-state, here. This strong field strength can inject carriers into the gate oxide. There are several RESURF-techniques to **re**duce this **sur**face **f**ield strength:

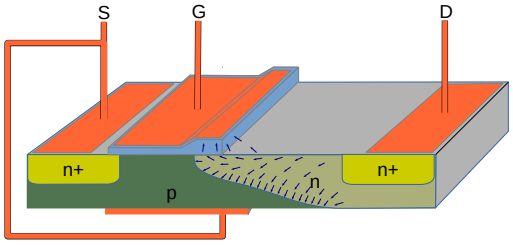

Fig. 7. Lateral NMOS with resurf

Such devices can block high voltages, but the thickness of the n-drift region is low which makes this structure less attractive for high currents. To obtain devices with high current capabilities, a vertical structure is much more suitable:

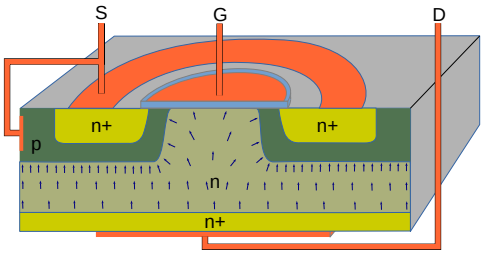

Fig. 8. Vertical NMOS

D. Temperature stability

An other effect of wide bandgap is a higher temperature stability. The temperature region, where semiconductors can opperate is limited. There is a certain minimum temperature (T_1) for the donator element's electrons to be in conduction band and a maximum temperature (T_2), also called intrinsic temperature, when the electrons of the intrinsic material can switch to the conduction band and make semiconductor operation impossible.

Due to the wide band gap, more thermal energy is required for

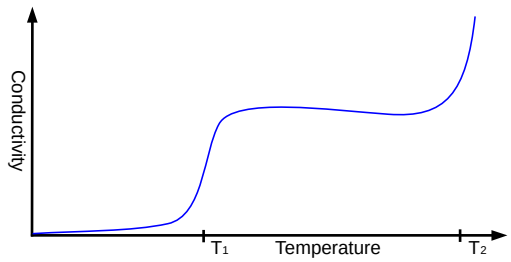

Fig. 9. Semiconductor opperating temperature[13]

electrons to jump into the conduction band. Therefore, wide bandgap devices can theoretically opperate at much higher temperatures up to 900 C for SiC[5]; the intrinsic temperature is not longer the limitation. For many applications, SiC is promised to be the best material. SiC got little lower bandgap and electron moility, than GaN, but a much higher thermal conductivity that enables high power densities, even for large devices. SiC for bulk material is also by a factor of 10 cheaper than GaN[3]. This makes SiC the better material for high power applications. But for laptop SMPS, the surface temperature is the limitating factor, even existing SMPS using silicon transistors can operate at much higher temperatures than allowed for the surface. So SiC's higher thermal conductivity is of no interest and GaN with it's partly higher band gap and electron mobility is the preferred material for laptop SMPS. Just because the wide bandgap transistors are smaller and the power losses concentrate at less volume, higher temperature stability is helpful, but GaN can fit this requirements without difficulties.

III. Problems with application of GaN

The reasons, why GaN devices needed such long time, to be marketable are fixed in difficulties with growing GaN crystals. GaN crystals tend to have a high density of point defects[20], are unflexible, and got different thermal expansion coefficients, than silicon. Therefore it is difficult, to grow a highly doped, crack-free GaN crystal.

A. Expensive bulk material

GaN bulk costs 100 €/cm^2 which is extremly expensive compared to silicon, which costs only 0.1 €/cm^2. So during the last years, a lot of effort was spent, to grow GaN on silicon wavers[15]-[17]. The difficulties here are for example the different thermal expansion coefficients of GaN and Silicon. This problem is also getting worse through the opportunity of GaN, to operate at high temperatures. But since there is a reliable Si-GaN contact, lateral GaN devices, where just a thin layer below the surface is made of GaN, became marketable. For vertical devices, a GaN bulk is required, so such devices where only produced for research.

B. Gate driver

One important fact on high efficient power transistors is, that switching losses are mainly caused by current flowing between drain and source, while the channel ist not completely established. The smaller gate capacity of GaN devices can reduce this critical switching duration, but the current for loading the gate is limited by gate and source impedances. It is task of an advanced gate driver to generate extremely short and powerful current pulses, that can load the MOSFET's gate completely. Such current pulses are mainly inhibited by the wiring inductivity between gate and driver. One option to keep this inductivity low is to place the driver on the same chip like the power transistor. Especially for rise time, advanced gate drivers prefetch the necessary energy within a special inductor, that can transfere this energy as fast as possible to the gate.[18] Such circuits are resonators where the energy commutes between gate and driver. To really optimize such gate drivers it is again helpfull, that power transistor and driver are on the same chip to have constant conditions regarding parasitic impedances.

C. No plasma devices

So called plasma devices, such as bipolar diodes, BJTs or IGBTs work with minority carrier currents. Because of the wide bandgap, the threshold voltage of PN-junctions is high, what makes diodes less attractive for lower voltages. The minority carrier livetime of GaN is also short, what results in bad amplification factors for BJTs. But for the regarded, unipolar FETs, this is not a problem.

D. No gate oxide

The miss of vertical devices is not the only problem, when building GaN MOSFETs. There is also no gate oxide with GaN. The dielectric has to be built with aluminium oxide[22] or silicon nitride which increases the complexity of production process.

IV. High Electron Mobility Transistor

Especially when regarding GaN, there is an exotic type of semiconductor devices, called High Electron Mobility Transistor (HEMT). Alloying GaN with Aluminium yields a new semiconductor material called AlGaN with a higher fermi level. Connecting GaN and AlGaN layers results in a Schottky contact. The space charge region behaves like an electron gas, where a high density of carriers having high mobility can move parallel to the contact. This is called two-dimensional electron gas (2DEG). On a GaN HEMT, the channel is made of such a 2DEG and therefore common HEMTs are normally on, and behave alike JFETs. There are different designs and material combinations for HEMTs, but the principal looks like this:

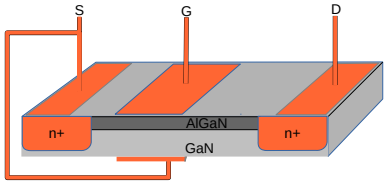

Fig. 10. JFET alike HEMT

There are two major problems regarding this design:

- The channel at the AlGaN-GaN contact is established by default, a gate to source voltage is required to deplete the channel and to turn the device off.
- The gate is not insulated, a certain gate current is flowing, and the gate is insufficiently protected from overvoltage or avalanche breakdowns. This makes the design of gate drivers much more complicated.

A. Normally-off, insulated gate HEMT

There is a big challenge of building enhancement mode, insulated gate HEMTs for being used like MOSFETs. The insulation is difficult for the same reason as it is on (MOS)FETs: The miss of a natural GaN gate oxide. To get the enhancement mode, different techniques are mentioned: Depleting the channel using a p-doped gate, making the AlGaN below the gate extremly thin to inhibit the 2DEG generation or to interrupt the channel with an insulated gate and use inversion channel for turning the device on.[23] An other option ist to use a cascode of a normally-on HEMT and a low voltage, normally-off Si-MOSFET.
But even, if there are enhancement mode GaN devices or workarounds, best efficiency is still achieved with the normally-on HEMTs.[19]

CONCLUSION

The higher voltage blocking capability of wide bandgap materials allows building of switching devices having low on-resistance and low gate capacity for higher efficiency and/or higher frequency. For building low power devices like a laptop SMPS that converts from 230 V AC to 19.5 V DC, GaN (not SiC) is the preferred material. In this case, the new GaN switches have to work together with conventional Si devices on the low voltage side. Most marketable GaN devices are optimized for voltages higher than 600 V and currents of several amperes. There are none or just a few low voltage devices between 200 and 600 V and currents less than 1 A. By using strongly overdimensioned switches, the efficiency benefit is not completely exploited. When designing a SMPS, the transformator operating voltage is arbitrary, because an active entrance rectifier (PFC) can boost as well as drop its output voltage. To decide for a certain design and voltage level, a comprehensive knowledge of technologies and market is required.

APPENDIX

TABLE I
COLLECTION OF IMPORTANT MATERIAL PARAMETERS:

Name	Letter	Unit	Value (Si)	Value (GaN)	Reference
intrinsic atom/molecule density	N	1/cm^3	$0.4993 \cdot 10^{23}$	$0.4388 \cdot 10^{23}$	[24]
bandgap	E_g	eV	1.12	3.45	[6]
electron affinity	E_e	eV	1.38	4.1	[11]
electron mobility	μ_n	cm^2/Vs	1500	1250	[13]; [7]
hole mobility	μ_p	cm^2/Vs	600	850	[13]; [7]
effective electron mass	$m^*{}_n$		$1.18 \cdot m_0$	$0.2 \cdot m_0$	[13]; [11]
effective hole mass	$m^*{}_p$		$0.81 \cdot m_0$	$0.8 \cdot m_0$	[13]; [11]
eq. density of conduction band states	N_c	1/cm^3	$3.3 \cdot 10^{19}$	$4.6 \cdot 10^{19}$	[10]
eq. density of valence band states	N_v	1/cm^3	$1.8 \cdot 10^{19}$	$2.3 \cdot 10^{18}$	[10]
electron ionization coefficient param.	a_n	1/cm^3	$1.1 \cdot 10^6$	$1.5 \cdot 10^5$	[14]; [12]
electron ionization coefficient param.	b_n	V/cm^3	$1.46 \cdot 10^6$	$1.413 \cdot 10^7$	[14]; [12]
hole ionization coefficient param.	a_p	1/cm^3	$2.1 \cdot 10^6$	$6.4 \cdot 10^5$	[14]; [12]
hole ionization coefficient param.	b_p	V/cm^3	$2.2 \cdot 10^6$	$1.454 \cdot 10^7$	[14]; [12]
dielectric constant	ϵ_r		12.5	9 ... 5.35 (HF)	[11]

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